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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,905	07/07/2003	Sergio Camerlo	CISCO-6920	7936

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EXAMINER	
KIM, AHSHIK	

ART UNIT	PAPER NUMBER
2876	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,905	CAMERLO ET AL.	
	Examiner	Art Unit	
	Ahshik Kim	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/3/05 (Amendment)*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. Receipt is acknowledged of the amendment filed on October 3, 2005. In the amendment claims 1, 15, 18, and 28, were amended, and claims 35 and 36 were newly added. Currently, claims 1-36 remain in the examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-3 and 10, 15-21, 28, 35, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani et al. (US 6,282,100 B1, hereinafter "Degani").

Re claims 1, 3, 15-21, 28, 35, and 36, Degani discloses an electronic interconnection system comprising printed wiring boards 15 and 21, a chip package 11 mounted on the PWB 15; the chip package has a first surface having contact pads (lower part of the chip package 11); an electrical connection in the form of solder balls connecting the chip package 11 with the PWB 15; and bridge lead 25 connecting the PWB 15 to the second PWB 21. As it not shown in the main figure, the runners 17 of figure 2 severs as connecting the chip with the wire bonding pads (end point of 25 on PWB 15). Therefore, a package substrate 18 of the instant application is 15 of Degani; and contacting pads 22 are the runners 17 of Degani.

Re claim 2, the chip 11 is mounted on the second surface of the PWB 15.

Degain discloses that the PWB 15 and PWB 21 are die bonded. It is the Examiner's view that die bonding and bonding utilizing solder ball are functionally well-known means of connecting electronic components. Degani, and many other cited references, in their disclosure, readily use die-boding, solder ball connection, and wire bonding in creating IC chip pagkage (see figure 3 of Degani). Accordingly, it is well within one ordinary skill in the art to incorporate solder bonding in connecting the chip package with PWB.

5. Claims 4-7, 11, 12, 22-25, and 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani et al. (US 6,282,100 B1) in view of Eldridge et al. (US 6,336,269, hereinafter "Eldridge).

The teachings of Degain have been discussed above. Degani, however, fails to specifically teach or fairly suggest the bridge lead is one of flying lead style, edge wiping style, top wiping style, or double wiping style.

Eldridge teaches an electronic component structure and various contact types used in manufacturing the electronic components (see abstract). The electronic components include PCB (col. 4, lines 14+) and electronic packages (col. 4, lines 65+). Eldridge further discloses various connecting means such as flying lead wire boding (col. 6, lines 51+) and wiping contact surface (col. 7, lines 2+).

In view of Eldridge's, disclosure, various bonding means such as flying lead style or wiping style are functionally equivalent means of connecting electronic components. What method is selected largely depends on the characteristics/functions of the component, production cost, availability of material, setup of manufacturing environment or purely the user's preference. Accordingly, it is the Examiner's view that choosing a particular method over the others would not affect the function of the electronic component.

6. Claims 8, 9, 13, 14, 26, 27, 33, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani et al. (US 6,282,100 B1) in view of Mertol (US 5,866,943, hereinafter "Mortel").

The teachings of Degain have been discussed above. Degani, however, fails to specifically teach or fairly suggest the bridge lead is comprised of means to dissipate heat and shielding electro-magnetic shields.

Mertol discloses an electronic package comprising an IC chip and ball grid array (see abstract). The packaged device includes electro-magnetic shielding. Some leads connected to the chip are connected to the heat sink to dissipate heat generated from the electronic package (col. 8, lines 23+).

In view of Mortels' disclosure, it would have been obvious to an ordinary skill in the art at the time the invention was made to employ notoriously well-known heat sink and electro-magnetic shielding to the teachings of Degani in order to ensure that the package's durability and desired functionalities are met. It is known that IC chips or packages generate heat, which needs to be transferred out to avoid overheating and a potential destruction of the chip. Various means of heat dissipating means are used in IC chip packages. Electro-magnetic interferences are often called "noise" which interferes with signal transmission from/to the chip to other devices. Means to reduce noise for the correct signal transmission is also readily used in chip manufacturing. These improvements would have been an obvious expedient, well within the ordinary skill in the art.

Response to Arguments

7. Applicant's amended claims and arguments filed on October 3, 2005 have been carefully reviewed and considered, but they are not persuasive.

Applicant argues that Degani reference disclosed a die-bonding between the PWB 15 and 21, and therefore it teaches away from electrical connection such as use of solder balls. Examiner respectfully disagrees. As shown in the main figure of Degani, solder ball bonding is used between the components 11 and 15; 21 and 28, and a die-bonding used between 15 and 25. Accordingly, it is the Examiner's view that it is obvious to one ordinary skill in the art to choose a particular bonding method desired between the components. Selection of bonding method may be based on issues such as cost, ease of manufacture and a circuit design.

Although the grounds of rejection have changed on some claims, it is the Examiner's belief that no new reference is introduced to support the Examiner's opinion.

The amended claims and remarks describing these elements have been fully considered, but they are not persuasive, and therefore, the Examiner has made this Office Action final.

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Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

10 A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

15 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

I. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Fehr et al. (US 2004/0067606); Karnezos (US 6,972,481); Shibue (US 6,958,259); Stewart et al. (US 6,906,425) disclose electronic interconnection system.

II. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ahshik Kim whose telephone number is (571)272-2393. The examiner can normally be reached between the hours of 6:00AM to 3:00PM Monday thru Friday. The fax number directly to the Examiner is (571)273-2393.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee, can be reached on (571)272-2398. The fax phone number for this Group is (703)872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [ahshik.kim@uspto.gov].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Ahshik Kim
Primary Examiner
Art Unit 2876
January 9, 2006